



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,291	03/29/2004	Jerome J. Cartmell	EMS-06601	2259
7590	03/23/2006		EXAMINER	
Patent Group Choate, Hall & Stewart Exchange Place 53 State Street Boston, MA 02109-2804			VO, THANH DUC	
			ART UNIT	PAPER NUMBER
			2189	
			DATE MAILED: 03/23/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/812,291	CARTMELL ET AL.
	Examiner Thanh D. Vo	Art Unit 2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 03 November 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-20 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 29 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>11/03/04</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. This Office Action is responsive to the Application filed on March 29, 2004.

Claims 1-20 are presented for examination. Claims 1-20 are pending.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on November 3, 2004 was filed after the mailing date of the Application on March 29, 2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 10-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The term "computer software" is directed to a non-statutory subject matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-6 and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (2004/0205384) in view of Pitts (6,052,308).

As per claims 1 and 10, Lai et al. disclosed a method of accessing data memory, comprising:

writing data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored (see page 2, par. 0024 and page 3, par. 0042, lines 1-10);

in response to a request to read data from the memory address, reading data from the first memory location or the second memory location (see page 3, paragraph 0042, lines 8-13); and

accessing data from the second memory location in response to a request to access data at the memory address when memory hardware corresponding to the first memory location has failed. See page 3, paragraph 0042, lines 10-13.

Lai et al. failed to teach the method of reading data from the memory locations based on load balancing. However, Pitts disclosed a method of reading the memory locations based on the load balancing (col. 5, lines 58-60). It would have been obvious to one having an ordinary skill in the art at the time of the invention to modify the system of Lai et al. to combine with the method taught by Pitts. In doing so, it would provide a system with more operational flexibility as well improving the speed and data sensing performance as taught by Pitts in col. 4, lines 5-10.

As per claims 2 and 11, Lai et al. disclosed a method, wherein accessing the data memory includes requesting access to a specific one of the first and second memory locations. See page 3, par. 0042, lines 6-8.

As per claims 3 and 12, Lai et al. disclosed a method, wherein the memory address contains a portion that is common to both the first memory location and the second memory location. See Fig. 7, item 110, wherein the address of the first and second memory modules are the same.

As per claim 4, Lai et al. disclosed a method, wherein hardware coupled to the memory causes data written using the memory address to be automatically written to the first memory location and the second memory location. See Fig. 7, item 120 and Fig. 1, item 12, wherein memory controller is hardware device.

As per claims 5 and 13, Lai et al. disclosed a method, wherein software causes data written using the memory address to be written to the first memory location and the second memory location using a first set of commands that writes the data to the first memory location and a second set of commands that writes to the second memory location. See page 3, par. 0042, lines 1-10. Furthermore, first and second set of commands are an inherent feature since a command is required in order to trigger the storage location in each of the memory module.

As per claims 6 and 14, Lai et al. failed to teach a method, wherein load balancing includes toggling at least one variable between a first state and a second state and wherein data is read from the first location when the at least one variable is in the first state and from the second location when the at least one variable is in the second state.

Pitts disclosed a method of toggling in the multiplexer between the two different states so that the data accessing is balanced between the upper memory cell and the lower memory cell. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to recognize that it is advantageous to implement the load balancing method disclosed by Pitts into the system of Lai et al. to arrive at the invention claim in claims 6 and 14. The motivation of doing so is to provide a system with more operational flexibility as well improving the speed and data sensing performance as taught by Pitts in col. 4, lines 5-10.

5. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (2004/0205384) in view of Pitts (6,052,308) and further in view of Hartwell et al. (2005/0160311).

As per claim 7, Lai et al. disclosed a method, further comprising: coupling a director board to the memory (see Fig. 1, item 12); and Lai et al. and Pitts failed to teach coupling one of: a host (mainframe), a disk, and a communications link to the director board.

Hartwell et al. taught that a host, a disk, and a communication link are connected to the memory system comprising a controller (director). See page 6, paragraph 0065, lines 4-9, and lines 11-18.

Lai, Pitts, and Hartwell are from the same field of endeavor, memory managing system.

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to implement a host, disk, and communication into the system of Lai in order to arrive at the invention claim in claim 7. The motivation of doing so is enabling any system that requires fault tolerant memory to take the advantage of the system reliability and continuous performance as taught by Hartwell et al. in page 6, paragraph 0065 lines 1-4.

As per claim 8, Lai et al. substantially taught a method, further comprising: transferring data between the memory and the director board. See page 2, paragraph 0027, lines 4-6.

As per claim 9, although Lai et al. and Pitts did not explicitly disclosing a director board causing data to be transferred between the memory and one of: the host, the disk, and the communication link. However, Hartwell et al. disclosed a system comprising a host (mainframe), a disk, and a communication link connected to a controller (director). Therefore, it would be readily recognized by one having an ordinary skill in the art at the time of the Applicant's invention to realize that coupling a

host, disk, and communication link to the memory system comprising a memory controller inherently comprising a step of communicating among said components. The motivation of doing so is to let the host inherits the fault tolerant memory system and therefore, the memory controller will manage the data transferring between the memory modules with the respective disk drive, host, or communicating through a communication link to broadcast or sending the requested data from clients.

6. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al. (2004/0205384) in view of Hartwell et al. (2005/0160311) and further in view of Pitts (6,052,308).

As per claim 15, Lai et al. disclosed a system, comprising:
an internal volatile memory (see Fig. 3, item M1); and
a plurality of directors (See Fig. 2, items 23a-23n) coupled to the memory; and
wherein each of the directors access the memory by writing data to first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored (see page 2, par. 0024 and page 3, par. 0042, lines 1-10); and

in response to a request to read data from the memory address, the directors read data from the first memory location or the second memory location (see page 3, paragraph 0042, lines 8-13); and

the directors access data from the second memory location in response to a request to access data at the memory address when memory hardware corresponding to the first memory location has failed. See page 3, paragraph 0042, lines 10-13.

Lai et al. failed to teach a plurality of disk drives. However, Hartwell et al. teaches a data storage device comprising of disk drives (see page 6, lines 11-17). It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to realize that it is advantageous to include at least one of the disk drive since the disk drive can be used to store software or firmware as taught by Hartwell et al. in page 6, lines 11-12.

Lai further failed to teach the directors are coupled to the disk drive and some of the directors are allow external access to the data storage device. However, Hartwell et al. teach a director (Fig. 1, item 108) that coupled to the disk drives said forth in the previous paragraph. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to recognize that coupling directors to disk drives and allow the external access to the storage device is known in the computer art. In doing so, the method of data transferring is greatly improved since the director (controller) is managing the data access being executed by the central processor and communicate with the external components as taught by Hartwell in page 4, paragraph 0042, lines 1-14.

Furthermore, Lai et al. failed to teach the method of load balancing access request to the memory. However, Pitts disclosed a method of reading the memory location based on the load balancing (col. 5, lines 58-60). It would have been obvious

to one having an ordinary skill in the art at the time of the Applicant's invention to modify the system of Lai et al. to combine with the method taught by Pitts. In doing so, it would provide a system with more operational flexibility as well improving the speed and data sensing performance as taught by Pitts in col. 4, lines 5-10.

As per claim 16, Lai et al. disclosed a system, wherein the directors request access to a specific one of the first and second memory locations. See page 3, par. 0042, lines 6-8.

As per claim 17, Lai et al. disclosed a system, wherein the memory address contains a portion that is common to both the first memory location and the second memory location. See Fig. 7, item 110, wherein the address of the first and second memory modules are the same.

As per claim 18, Lai et al. disclosed a system, wherein hardware coupled to the memory causes data written using the memory address to be automatically written to the first memory location and the second memory location. See Fig. 7, item 120 and Fig. 1, item 12, wherein memory controller is hardware device.

As per claim 19, Lai et al. disclosed a system, wherein software causes data written using the memory address to be written to the first memory location and the second memory location using a first set of commands that writes the data to the first

memory location and a second set of commands that writes to the second memory location. See page 3, par. 0042, lines 1-10. Furthermore, first and second set of commands are an inherent feature since a command is required in order to trigger the storage location in each of the memory module.

As per claim 20, Lai et al. failed to teach a method, wherein load balancing includes toggling at least one variable between a first state and a second state and wherein data is read from the first location when the at least one variable is in the first state and from the second location when the at least one variable is in the second state.

Pitts disclosed a method of toggling in the multiplexer between the two different states so that the data accessing is balanced between the upper memory cell and the lower memory cell. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to recognize that it is advantageous to implement the load balancing method disclosed by Pitts into the system of Lai et al. to arrive at the invention claim in claim 20. The motivation of doing so is to provide a system with more operational flexibility as well improving the speed and data sensing performance as taught by Pitts in col. 4, lines 5-10.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

h
Thanh Vo
Patent Examiner
Art Unit: 2189
3/16/2006

Reginald M. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER